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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/972,855	10/10/2001	Yoshiaki Sugizaki	04329.2686	5564

7590 04/05/2005  
Finnegan, Henderson, Farabow  
Garrett & Dunner, L.L.P.  
1300 I Street, N.W.  
Washington, DC 20005-3315

EXAMINER

IM, JUNGHWA M

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/972,855

Applicant(s)

SUGIZAKI, YOSHIAKI

Examiner

Junghwa M. Im

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,2,4-11,14-18 and 21-25 is/are pending in the application.
- 4a) Of the above claim(s) 1,2,4-11 and 14-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 21-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____  |

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 13, 2005 has been entered.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 21-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsuan (US 6429509).

Regarding claim 21, Fig. 3C of Hsuan shows a semiconductor device comprising:

a first semiconductor chip [300(1)] where a semiconductor element is formed (an active area above the dashed line);

a plurality of first connecting terminals (connecting bumps ) arranged on a semiconductor element formation surface side in the first semiconductor chip, and connected electrically to the

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semiconductor element, the first connecting terminals having substantially the same configuration;

a plurality of conductive members [417 in Fig. 4K] buried in a plurality of through holes that go through the first semiconductor chip; and

a plurality of second connecting terminals (connection bumps) arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive members, wherein at least either the first connecting terminals or the second connecting terminals is coupled to an assembly board (col. 5, lines 35-44; col. 10, lines 11-18), and

some of the first connecting terminals or the second connecting terminals are distributed and arranged substantially on an entire surface of the semiconductor chip, and a power source supply potential or ground potential is to be applied to said some of the first or second connecting terminals (col. 5, lines 21-44).

Regarding claim 22, Fig. 3C of Hsuan shows a second semiconductor chip [300(2)] stacked on the first semiconductor chip, wherein at least portion of the connecting terminals arranged on a stacked surface between the first semiconductor chip and the second semiconductor chip of the first connecting terminals and the second connecting terminals in the first semiconductor chip is coupled to the second semiconductor chip (through interconnecting two chips to form an integrated circuit; col. 7, lines 13-45).

Regarding claim 23, Fig. 3C of Hsuan shows a semiconductor device further comprising a second to an n-th (wherein n is a positive integer of three or more) semiconductor chips stacked above first semiconductor chip, wherein at least a portion of the connecting terminals arranged

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on a stacked surface between the first semiconductor chip and the second semiconductor chip of the first connecting terminals and the second connecting terminals in the first semiconductor chip is coupled to the second to n-th semiconductor chips (col. 7, lines 13-45).

Regarding claim 24, Fig. 4D of Hsuan shows a semiconductor device wherein said at least a portion of the plurality of connecting terminals comprises conductive bumps.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsuan in view of Dore et al. (US 6239484), hereinafter Dore.

Regarding claim 25, Fig. 3C of Hsuan shows a semiconductor device comprising:

a first semiconductor chip [300(1)] where a semiconductor element is formed;

a plurality of first connecting terminals (connecting bumps) arranged on a semiconductor element formation surface side (an active area above the dashed line) in the first semiconductor chip, and connected electrically to the semiconductor element the first connecting terminals having, substantially the same configuration;

a plurality of conductive members [417 in Fig. 4K] buried in a through hole that goes through the first semiconductor chip;

a plurality of second connecting terminal terminals arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive members (col. 7, lines 13-45);

a second semiconductor chip [300(2)] stacked on the first semiconductor chip;

a plurality of third connecting terminal terminals arranged on a semiconductor element formation surface side in the second semiconductor chip, wherein one of the first connecting terminals and the second connecting terminals of the first semiconductor chip is arranged at a position facing the third connecting terminals of the second semiconductor chip, the first semiconductor chip and the second semiconductor chip are electrically connected with each other through the facing connecting terminals,

some of the first connecting terminals or the second connecting terminals are distributed and arranged substantially on an entire surface of the semiconductor chip, and a power source supply potential or ground potential is to be applied to said some of the first or second connecting terminals (col. 5, lines 21-44).

Fig. 3C of Hsuan shows most aspect of the instant invention except "the second semiconductor chip is thicker or larger than the first semiconductor chip." Fig. 3 of Dore shows a semiconductor device wherein the second semiconductor chip/ an upper chip thicker or larger than the first semiconductor chip/a lower chip.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Dore into the device of Hsuan in order to the second semiconductor chip/ an upper chip thicker or larger than the first semiconductor chip/a lower chip to accommodate the design specification.

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*Response to Arguments*

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.


*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

  
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